WHAT IS CLAIMED IS:

1. A circuit for providing a reduced harmonic content output signal that is modulated according to an input signal, the circuit comprising:

an oscillator circuit including at least one circuit portion configured to receive first and second orthogonal oscillator input signals having respective first and second phases, and to provide plural oscillator output signals having respective mutually distinct phases that are interpolated between the first and second phases; and

a harmonic rejection mixer configured to use the input signal to modulate a combination of the oscillator output signals, the oscillator output signals being respectively weighted so as to provide an emulated sinusoidal signal constituting the reduced harmonic content output signal.

2. The circuit of Claim 1, wherein:

the oscillator circuit is configured to provide the oscillator output signals in response to only a first pair of orthogonal oscillator input signals and a second pair of orthogonal oscillator input signals that are opposite in phase to the first pair of orthogonal oscillator input signals.

3. The circuit of Claim 2, wherein:

the oscillator input signals are of a same frequency as the oscillator output signals, and are not derived from a frequency-division of higher frequency oscillator input signals

4. The circuit of Claim 1, wherein at least one of the circuit portions (FIG. 2A) includes:

at two phase interpolation circuits, each phase interpolation circuit being configured to provide a respective one of the oscillator output signals by combining at least two weighted oscillator input signals.

5. The circuit of Claim 1, wherein the oscillator circuit includes exactly four circuit portions, including:

a first circuit portion receiving I and Q- orthogonal oscillator input signals;

a second circuit portion receiving I and Q orthogonal oscillator input signals;

a third circuit portion receiving I- and Q orthogonal oscillator input signals; and

a fourth circuit portion receiving I- and Q- orthogonal oscillator input signals;

and wherein:

I and I- are of opposite phase; and

Q and Q- are of opposite phase.

6. The circuit of Claim 5, wherein:

the first circuit portion provides at least first and second oscillator output signals having first and second phases interpolated between phases of I and Q-;

the second circuit portion provides at least third and fourth oscillator output signals having first and second phases interpolated between phases of I and Q;

the third circuit portion provides at least fifth and sixth oscillator output signals having first and second phases interpolated between phases of I- and Q; and

the fourth circuit portion provides at least seventh and eighth oscillator output signals having first and second phases interpolated between phases of I- and Q-.

7. The circuit of Claim 6, wherein:

the first circuit portion provides a ninth oscillator output signal having a phase substantially matching that of one of the I or Q- orthogonal oscillator input signals;

the second circuit portion provides a tenth oscillator output signal having a phase substantially matching that of one of the I or Q orthogonal oscillator input signals;

the third circuit portion provides an eleventh oscillator output signal having a phase substantially matching that of one of the I- or Q orthogonal oscillator input signals; and

the fourth circuit portion provides a twelfth oscillator output signal having a phase substantially matching that of one of the I- or Q- orthogonal oscillator input signals.

8. The circuit of Claim 1, wherein:

the oscillator output signals are equally spaced in phase.

9. The circuit of Claim 1, further comprising:

an array of load equalization buffers configured to weight the oscillator output signals in accordance with a strength of legs forming the harmonic rejection mixer, the strength of the legs being determined by how much each leg contributes to the reduced harmonic output signal.

10. The circuit of Claim 1, wherein at least one of the circuit portions includes:

at two phase interpolation circuits, each phase interpolation circuit being configured to provide a respective one of the oscillator output signals by performing a weighted summing of currents respectively representing at least two oscillator input signals.

11. A method for providing a reduced harmonic content output signal that is modulated according to an input signal, the method comprising:

receiving first and second orthogonal oscillator input signals having respective first and second phases;

providing plural oscillator output signals having respective mutually distinct phases that are interpolated between the first and second phases; and

using the input signal to modulate a combination of the oscillator output signals, respectively weighted so as to provide an emulated sinusoidal signal constituting the reduced harmonic content output signal.

12. The method of Claim 11, wherein the providing step includes:

providing the oscillator output signals in response to only a first pair of orthogonal oscillator input signals and a second pair of orthogonal oscillator input signals that are opposite in phase to the first pair of orthogonal oscillator input signals.

13. The method of Claim 12, wherein:

the oscillator input signals are of a same frequency as the oscillator output signals, and are not derived from a frequency-division of higher frequency oscillator input signals

14. The method of Claim 11, wherein the providing step includes:

providing the oscillator output signals by combining at least two weighted oscillator input signals.

15. The method of Claim 11, wherein the receiving step consists essentially of:

receiving I and Q- orthogonal oscillator input signals;

receiving I and Q orthogonal oscillator input signals;

receiving I- and Q orthogonal oscillator input signals; and

receiving I- and Q- orthogonal oscillator input signals;

and wherein:

I and I- are of opposite phase; and

Q and Q- are of opposite phase.

16. The method of Claim 15, wherein the providing step includes:

outputting at least first and second oscillator output signals having first and second phases interpolated between phases of I and Q-;

outputting at least third and fourth oscillator output signals having first and second phases interpolated between phases of I and Q;

outputting at least fifth and sixth oscillator output signals having first and second phases interpolated between phases of I- and Q; and

outputting at least seventh and eighth oscillator output signals having first and second phases interpolated between phases of I- and Q-.

17. The method of Claim 16, wherein the providing step includes:

outputting a ninth oscillator output signal having a phase substantially matching that of one of the I or Q- orthogonal oscillator input signals;

outputting a tenth oscillator output signal having a phase substantially matching that of one of the I or Q orthogonal oscillator input signals;

outputting an eleventh oscillator output signal having a phase substantially matching that of one of the I- or Q orthogonal oscillator input signals; and

outputting a twelfth oscillator output signal having a phase substantially matching that of one of the I- or Q- orthogonal oscillator input signals.

18. The method of Claim 11, wherein the providing step includes:

providing the oscillator output signals equally spaced in phase.

19. The method of Claim 11, further comprising:

weighting the oscillator output signals in accordance with a strength of legs forming a harmonic rejection mixer that performs the using step, the strength of the legs being determined by how much each leg contributes to the reduced harmonic output signal.

20. The method of Claim 11, wherein the providing step includes:

providing the oscillator output signals by performing a weighted summing of currents that respectively represent at least two oscillator input signals.